

Measured Propagation Characteristics of Finite Ground Coplanar Waveguide on Silicon with a Thick Polyimide Interface Layer

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Abstract—*Measured propagation characteristics of Finite Ground Coplanar (FGC) waveguide on silicon substrates with resistivities spanning 3 orders of magnitude (0.1 to 15.6 Ohm cm) and a 20 nm thick polyimide interface layer are presented as a function of the FGC geometry. Results show that there is an optimum FGC geometry for minimum loss, and silicon with a resistivity of 0.1 Ohm cm has greater loss than substrates with higher and lower resistivity. Lastly, substrates with a resistivity of 10 Ohm cm or greater have acceptable loss characteristics.*

INTRODUCTION

Radio Frequency and Microwave Monolithic Integrated Circuits (RFICs and MMICs) fabricated on silicon substrates have obtained widespread use in personal communication, GPS, and other systems that are highly dependent on cost. While some of this market is due to reductions of CMOS gate width, the rest of it is due to the development of SiGe Heterojunction Bipolar Transistors (HBTs). Both of these technologies have pushed the frequency range of silicon RFICs to X-Band for commercial parts and Ka-Band and V-Band for research circuits. However, transmission lines and passive circuit components fabricated directly on standard, low-resistivity silicon wafers commonly used in commercial foundries have high loss, or low Q-factors [1]. Therefore, the transmission lines and passive components must be designed to shield the electric fields from the silicon as is done in thin film microstrip lines [2], or the field interaction with the silicon must be reduced by the use of insulators that separate the metal lines from the silicon [3-4]. Figure 1 shows a Finite Ground Coplanar (FGC) line fabricated on silicon with a polyimide interface layer, which lifts the transmission line off of the silicon wafer and minimizes field interaction.

The FGC line shown in Figure 1 may be thought of as a Metal-Insulator-Semiconductor (MIS)

structure that may support three modes of propagation (skin effect mode, a dielectric quasi-TEM mode, and a slow-wave mode), and prior work on MIS coplanar waveguides has explored this with the goal of developing slow wave structures for circuits size reduction [5-7]. However, the slow-wave structures were built on thin insulators deposited over a thin, highly doped semiconductor layer that is grown on an insulating material [5,6]. Because the insulating layer is thin (less than 1 μm), the fields interact strongly with the semiconductor layer and the attenuation is reported to be greater than 10 dB/cm [6,7]. Thus, while interesting and useful for some purposes, the attenuation is too high for most Si RFICs. While references [3] and [4] demonstrated the viability of using thick polyimide interface layers to reduce the dielectric loss of FGC lines and Coplanar Waveguides (CPW) on low resistivity silicon wafers, they did not investigate the influence of the substrate resistivity on the transmission line propagation characteristics. Furthermore, the design rules that were presented do not necessarily yield the lowest attenuation constant.

In this paper, we present for the first time measured characteristics of FGC lines built on a thick, polyimide interface layer deposited on Si wafers with resistivities that span 0.1 to 15.6 Ohm cm, which covers the range commonly used in

CMOS and BiCMOS circuit fabrication. The results are presented to yield design rules for choosing the optimum substrate resistivity and FGC line dimensions.

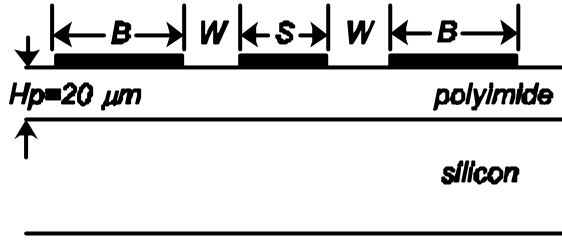


Figure 1: Cross-sectional cut of Finite Ground Coplanar (FGC) waveguide fabricated on a silicon wafer with a thick, polyimide interface layer.

CIRCUIT FABRICATION AND CHARACTERIZATION

The resistivity of silicon substrates from three different wafer lots were first measured with a four-point probe and determined to be 0.1, 1.8, and 15.6 Ohm cm. These wafer lots were purposely chosen to encompass the resistivity values commonly used in CMOS and BiCMOS circuits. Dupont adhesion promoter and four, 5 μm thick layers of Dupont PI-2611 polyimide were spun onto the wafer to yield a total polyimide interface layer thickness of 20 μm . Each layer of polyimide was fully cured at 340 C for 120 minutes before the next layer was added. PI-2611 polyimide has a relative dielectric constant of 3.12 measured at 1 MHz [8] and a loss tangent of 0.002 measured at 1 kHz [9]. The metal FGC circuit consists of 200 Å Ti and 1.5 μm of evaporated Au, both of which are defined by a liftoff process.

The circuits for measuring the propagation constant, $\gamma = \alpha + jk_0\sqrt{\epsilon_{\text{eff}}}$ where α is the attenuation constant and ϵ_{eff} is the effective permittivity, consist of Thru-Reflect-Line (TRL) calibration standards with four delay lines of 850, 1700, 3500, and 10000 μm to cover the frequency band of 1 to 50 GHz. The TRL calibration was implemented with MULTICAL [10], a TRL software program that computes the propagation constants of the lines by using the difference in the measured magnitude and phase between the thru and delay lines. To improve accuracy, each circuit was measured several times and the average of those measurements are presented in this paper. The measurements were performed on a vector network analyzer and a microwave probe station. While probing, a thick quartz plate was

placed between the silicon wafer and the metal wafer chuck, but measurements confirmed that this did not have a measurable influence on the propagation constant.

Sonnet 2-D simulation software was used to choose FGC line dimensions that yield 50 Ohm characteristic impedance on 15.6 Ohm cm silicon with the 20 μm thick polyimide interface layer. Simulations showed that the characteristic impedance reduced as the resistivity reduced, but within reasonable engineering approximation, the impedance of the lines on all of the substrates may be assumed to be 50 Ohm. The dimensions of the FGC lines are shown in Table 1.

Table 1: Dimensions of FGC lines

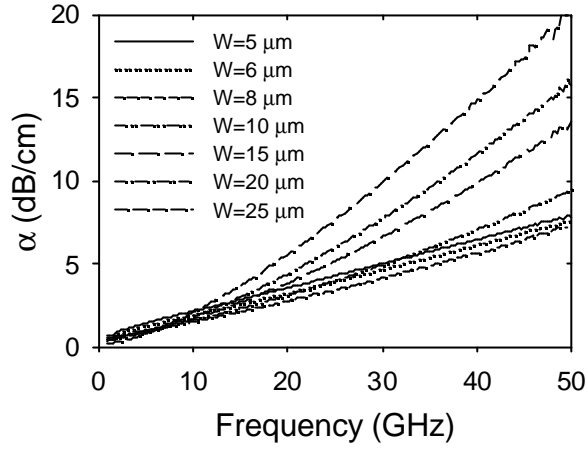
S (μm)	W (μm)	B=3S (μm)	S+2W (μm)
51	5	153	61
62	6	186	74
74	8	222	90
90	10	270	110
114	15	342	144
120	20	360	160
140	25	420	190

The finite-difference time-domain (FDTD) technique was also used to model the FGC lines described in the second entry of Table 1, with $W=6\mu\text{m}$ and $S=62\mu\text{m}$. A numerical mesh of 104 by 132 by 75 cells terminated with 10 cells of Perfectly Matched Layer (PML) in each direction was used with a time step of $.99\Delta t_{\text{max}}$. A Gaussian derivative pulse with frequency content up to 50GHz was applied as a soft-source excitation. The results of those simulations are presented alongside the measurement results and show excellent agreement.

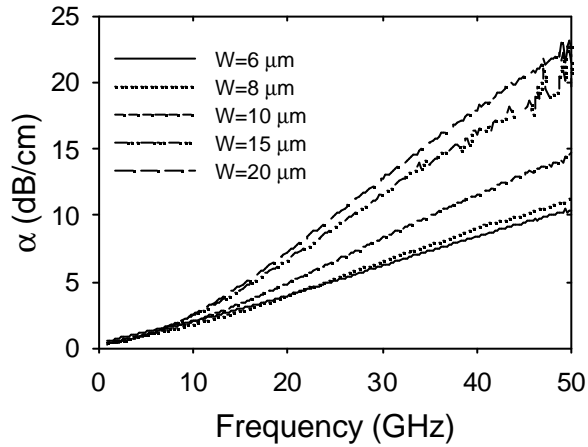
RESULTS

The measured attenuation of the FGC lines fabricated on the three silicon wafers is shown in Figure 2. It is seen that the frequency dependence of the attenuation is complicated and highly dependent on the silicon resistivity and FGC line dimensions. When the substrate resistivity is very low (0.1 Ohm cm), the frequency dependence of attenuation is modeled well by $\alpha = a f^b$ where f is the frequency and a and b are fitting parameters. If conductor loss dominated, b should be 0.5, but even for the narrowest slot width, $b=0.8$ and

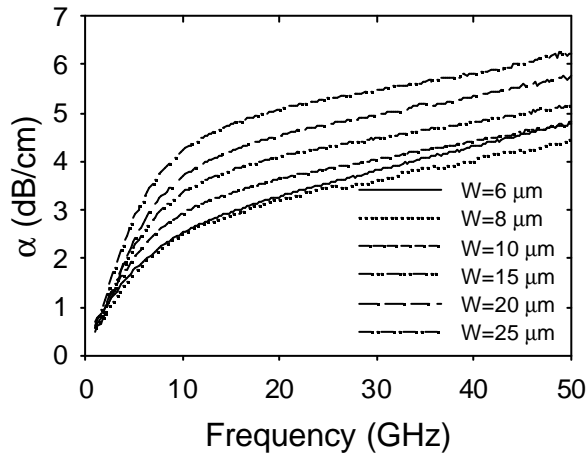
increases to 1.4 for the widest slot width, indicating dielectric attenuation is dominating. It is also noted that $b=1$ for the $W=8\ \mu\text{m}$ ($S+2W=90\ \mu\text{m}$) FGC line, which agrees with the design rule presented in [4].



(a) $\rho=0.1\ \text{Ohm cm}$



(b) $\rho=1.8\ \text{Ohm cm}$



(c) $\rho=15.6\ \text{Ohm cm}$

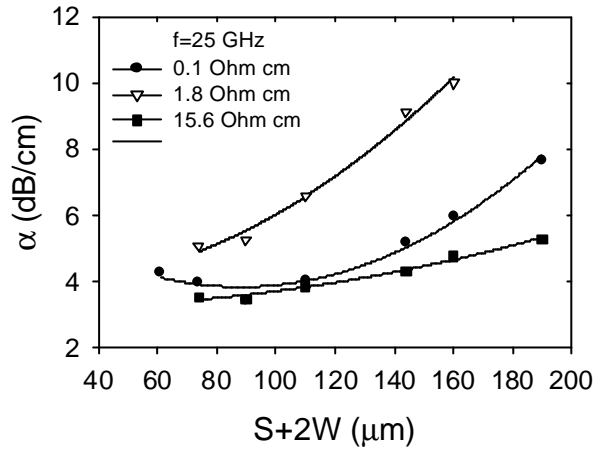
Figure 2 : Measured attenuation of FGC lines on silicon substrates with resistivities of (a) 0.1 Ohm cm, (b) 1.8 Ohm cm, and (c) 15.6 Ohm cm.

The 1.8 Ohm cm silicon substrate has similar frequency dependence, but inflection points are seen that indicate a more complicated frequency dependence. If the substrate resistivity is increased by another order of magnitude to 15.6 Ohm cm, the attenuation appears to be conductor loss dominated, but still indicating the influence of other loss mechanisms. In fact, $a = a f^b$ may not be used to model the attenuation.

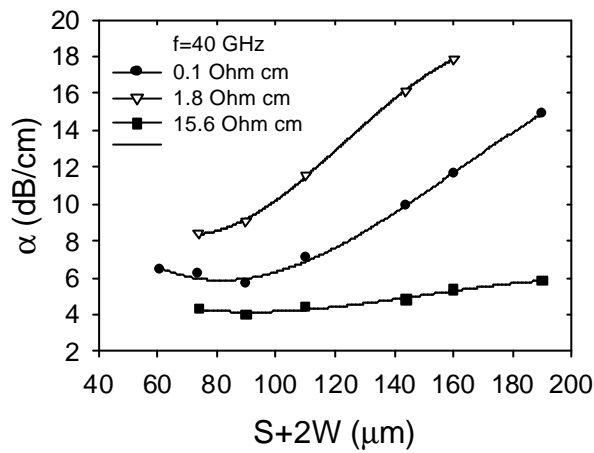
Using the information in Figure 2, the dependence of attenuation on the FGC line geometry and Si resistivity may be obtained. This is summarized in Figure 3, which shows the attenuation as a function of $S+2W$ with the Si resistivity as a parameter. As seen in Figure 3, for circuits in the microwave region, the FGC dimensions must be chosen to minimize the total loss, which is a combination of the conductor and dielectric loss. From Figures 3a and 3b, it is seen that $S+2W$ approximately equal to $90\ \mu\text{m}$ yields the minimum attenuation at both 25 and 40 GHz. This is the same value that yielded an approximately linear frequency dependence for low resistivity substrates, and yields a design rule of $(S+2W)/Hp=4$ for minimum insertion loss. For smaller line width, conductor loss is higher, but for wider lines, the electric field interaction with the silicon is greater, which increases dielectric loss. For low frequencies ($f \sim 1\ \text{GHz}$), it has been found that $S+2W$ should be maximized for low attenuation. Figure 3 also shows the interesting result that Si with a resistivity near 1 Ohm cm has higher attenuation than resistivities of 0.1 and 10 Ohm cm. A peak in attenuation over a range of substrate resistivity has been predicted for MIS coplanar lines with thin insulator and semiconductor layers [6], but the value of the resistivity for maximum attenuation is different in this case. Lastly, Figure 3 clearly shows that a substrate resistivity of 10 Ohm cm or greater is required for acceptable attenuation for a wide range of FGC line widths.

CONCLUSIONS

Measured propagation characteristics of FGC lines on silicon substrates of different resistivities with a polyimide interface layer are presented for the first time. Design rules are also derived for minimum line attenuation, for wafers with a resistivity between 0.1 and 15.6 Ohm cm.



(a)



(b)

Figure 3: Measured attenuation as a function of FGC line width and Si resistivity at (a) 25 GHz, and (b) 40 GHz.

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REFERENCES

- [1] G. E. Ponchak, "RF transmission lines on silicon substrates," *29th European Microwave Conference Dig.*, Munich, Germany, Oct. 5-7, 1999, pp. 158-161.
- [2] G. E. Ponchak and A. N. Downey, "Characterization of thin film microstrip lines on polyimide," *IEEE Trans. Components, Packaging, and Manufacturing Tech. -Part B*, Vol. 21, No. 2, pp. 171-176, May 1998.

- [3] G. E. Ponchak and L. P. B. Katehi, "Measured attenuation of coplanar waveguide on CMOS grade silicon substrates with a polyimide interface layer," *IEEE Electronics Letters*, Vol. 34, No. 13, pp. 1327-1329, June 25, 1998.
- [4] G. E. Ponchak, A. Margomenos, and L. P. B. Katehi, "Low loss CPW on low resistivity Si substrates with a micromachined polyimide interface layer for RFIC interconnects," *IEEE Trans. Microwave Theory and Techniques*, Vol. 49, No. 5, pp. 866-870, May 2001.
- [5] R. Sorrentino, G. Leuzzi, and A. Silbermann, "Characteristics of metal-insulator-semiconductor coplanar waveguides for monolithic microwave circuits," *IEEE Trans. Microwave Theory and Techniques*, Vol. 32, No. 4, pp. 410-416, April 1984.
- [6] Yoshiro Fukuoka, Yi-Chi Shih, and Tatsuo Itoh, "Analysis of slow-wave coplanar waveguide for monolithic integrated circuits," *IEEE Trans. Microwave Theory and Techniques*, Vol. 31, No. 7, pp. 567-573, July 1983.
- [7] Tsugumichi Shibata and Eiichi Sano, "Characteristics of MIS structure coplanar transmission lines for investigation of signal propagation in integrated circuits," *IEEE Trans. Microwave Theory and Techniques*, Vol. 38, No. 7, pp. 881-889, July 1990.
- [8] J. Leu, H.-M. Ho, J. K. Lee, J. Kasthurirangan, C. N. Liao, and P. S. Ho, "The evaluation of low dielectric constant materials for deep submicron interconnect applications," in *Proc. 6th Meeting Dupont Symp. Polyimide Microelectronics*, May 1-3, 1995.
- [9] Dupont Company Pyralin LX data sheet.
- [10] R. B. Marks, "A multilane method of network analyzer calibration," *IEEE Trans. Microwave Theory and Techniques*, Vol. 39, pp. 1205-1215, July 1991.